8. The circuit recited in claim 7, wherein said clock signal generator means supplies multi-phase clock signals.

9. The circuit recited in claim 6, wherein said clock signal generator means applies non-overlapping multi-phase clock signals to the respective control terminsla of said pair of field effect transistors, such that one of said transistors is rendered conducting while the other transistor is rendered non-conducting, and vice versa, for successively charging and discharging said capacitor.

10. The circuit recited in claim 1, wherein said clock signal generator means includes a crystal controlled oscillator.

11. THe circuit recited in claim 1, further comprising an RC low pass filter connected between the output terminal means and the first input terminal means of said operational amplifier means.

12. The circuit recited in claim 1, further comprising a resistor connected between a source of reference potential and the first input terminal means of said operational amplifier means to provide for offset compensation of the output terminal means of said operational amplifier means.

13. A capacitance-to-voltage converter circuit for providing an accurate measurement of the capacitance of a capacitor, said circuit comprising:

clock means for supplying a clock signal which alternates between relatively high and relatively low voltage levels;

operational amplifier means having input and output terminal means; and

means for successively charging and discharging said capacitor including a buffer amplifier interconnected between said clock means and one plate of said capacitor for charging said capacitor during a first portion of the clock signal, and multi-terminal semiconductor switch means interconnected between said operational amplifier means and the second plate of said capacitor for discharging said capacitor to the input terminal means of said operational amplifier means during a second portion of the clock signal;

the magnitude of the voltage at the output terminal means of said operational amplifier means providing a measurement of the capacitance of said capacitor.

14. The circuit recited in claim 13, wherein said clock means includes a crystal controlled oscillator.

15. The circuit recited in claim 14, wherein said clock means also includes a non-overlapping clock generator which is driven by the output of said crystal controlled oscillator.

16. The circuit recited in claim 13, wherein the input terminal means of said operational amplifier means comprises an inverting input terminal connected to said semiconductor switch means at a virtual ground and a non-inverting input terminal connected to ground.

17. The circuit recited in claim 16, wherein said semiconductor switch means comprises a pair of field effect transistors having their respective conduction paths connected in electrical series between the inverting input terminal of said operational amplifier means and ground, said clock means being connected to the respective control terminals of said pair of field effect transistors to control the operation thereof, and the second plate of said capacitor being connected to the series node between said pair of field effect transistors.

18. The circuit recited in claim 17, wherein said clock means also applies non-overlapping clock signals to the respective control terminals of said pair of field effect transistors, such that one of said transistors is rendered conducting while the other transistor is rendered non-conducting, and vice versa, for successively charging and discharging said capacitor.

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